THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 22

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte STEVEN A. HUNLEY

Appeal No. 95-0020
Application 08/052,213[1]

ON BRIEF

Before HAIRSTON, KRASS, and BARRETT, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 42 through 44 and 46. Claims 45, 47 and 48 have been indicated by the examiner as being directed to allowable subject matter but stand objected to as relying on a rejected base claim. Claims 8, 10 through 19, 22, 24 through 29 and 31 through 41 have been allowed.

[1] Application for patent filed April 23, 1993. According to appellant, this application is a continuation of Application 07/776,141, filed October 15, 1991.

The invention is directed to a CMOS buffer with a controlled slew rate. By optimally controlling the rate of transition from a high/low state to a low/high state at the output, reduction of signal line reflection and ringing at the output and in the cable or connectors coupled to the output is said to be enabled.

Independent claim 42 is reproduced as follows:

42. A method of controlling slew rate on an output terminal, comprising the steps of:

activating an output transistor;

comparing a voltage on the output terminal to an internal node voltage during output transistor activation; and

modulating the rate of a voltage transition at the output terminal in response to the comparison of the output terminal to the internal node voltage.

The examiner relies on the following reference:

Bianchi 5,122,690 Jun. 16, 1992
(filed Oct. 16, 1990)

Claims 42 through 44 and 46 stand rejected under 35 U.S.C. ' 102(e) as anticipated by Bianchi.

Reference is made to the brief and answer for the respective positions of appellant and the examiner.

OPINION

In accordance with appellant’s statement at page 3 of the brief, claims 42 through 44 and 46 stand or fall together. Accordingly, we will base our decision on an analysis of independent claim 42.

The examiner applies Figure 2 of Bianchi against instant claim 42 as follows:

The output transistor being activated is identified as transistor NS. Voltage on output terminal 50 is said to be compared to an internal node voltage (at the output of inverter 44) during activation of output transistor NS with the comparison effected by NOR gate 46, the result of such comparison either enabling or disabling transistor NL. The examiner then points to column 6, line 38, to column 7, line 8 of Bianchi for a teaching of modulating the rate of voltage transition at the output terminal in response to the comparison of the output terminal to the internal node voltage.

Appellant takes the position that Bianchi does not teach any "modulating" but that if it did, it certainly does not teach "modulating the rate of a voltage transition" and, even if one considered that Bianchi did teach such, Bianchi clearly does not teach this modulation step "in response to the comparison of the output terminal to the internal node voltage" as set forth in claim 42.

We agree with the examiner that claim 42 sets forth rather broad language. We also agree with the examiner that the term, "modulating," per se, is broad enough to cover an on/off situation as in Bianchi where transistor NL is disabled if a current condition exceeds some value.

However, instant claim 42 does not call for "modulating," per se, but rather for "modulating the rate of a voltage transition at the output terminal…" Notwithstanding the examiner's valiant, and commendable, effort to interpret the broad language of claim 42 in such a manner as to make Bianchi's disclosure applicable to such language, it is our view that Bianchi simply does not disclose or suggest the modulation of "the rate of a voltage transition." At best, perhaps one could say that an output voltage level in Bianchi is "modulated" by switching transistors on or off, based on current magnitude, but even this interpretation is one that views as a modulation the switching of an output voltage between two levels. Quite clearly, there is no modulation of a "rate of a voltage transition at the output terminal" [emphasis ours], as claimed, in the digital circuitry of Bianchi. We simply cannot agree with the examiner, at page 4 of the answer, that Bianchi's disabling of pulldown transistor NL "inherently 'modulates the rate of voltage transition' in that the disabling of the large transistor will slow down the transition of the output terminal from the previous logic high to a logical low."

Since we find that Bianchi's digital circuitry does not teach or suggest the claimed "modulating the rate of a voltage transition at the output terminal…," Bianchi cannot anticipate

the instant claimed invention. Accordingly, the examiner's decision rejecting claims 42 through 44 and 46 under 35 U.S.C. ' 102(e) is reversed.

REVERSED

Kenneth W. Hairston Administrative Patent Judge	)	
Errol A. Krass Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
Lee E. Barrett Administrative Patent Judge	)	

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